VMC Based Universal Motor

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Abstract- This paper introduces a new family of dc–dc converters based voltage multiplier cells. A brief literature review is presented to demonstrate some advantages and inherent limitations of several topologies that are typically used in voltage step-up applications. The analyzed converter can be applied in uninterruptible power supplies, fuel cell systems, and is also adequate to operate as a high-gain boost stage with cascaded inverters in renewable energy systems. In order to verify the operation principle of this family, the boost converter is chosen and investigated in detail. The behavior of the converter is analyzed through an extensive theoretical analysis. Furthermore, it is suitable in cases where dc voltage step-up is demanded, such as electrical fork-lift, audio amplifiers, and many other applications.

Index Terms—Boost converters, dc–dc converters, high voltage gain, voltage multiplier cells (VMCs).

INTRODUCTION

Depending on the application nature, several types of static power converters are necessary for the adequate functioning of the energy provided by primary sources such as photovoltaic arrays, wind turbines, and fuel cells. Besides, considering that the overall cost of renewable energy systems is high, the use of high-efficiency power electronic converters is a must [1],[10]. The literature presents numerous examples for applications where dc–dc step-up stages are necessary, e.g., audio amplifiers [2], uninterruptible power supplies (UPSs) [3], fuel cell powered systems [4], and fork lift vehicles [5], although many other ones can be easily found. Typical solutions include the use of low-frequency or high-frequency power transformers to adjust the voltage gain properly. Besides, galvanic isolation may be necessary due to safety reasons [6]. Unfortunately, this may bring increased size, weight, and volume if compared with nonisolated approaches such as the boost converter. The conventional boost converter can be advantageous for step-up applications that do not demand very high voltage gain, mainly due to the resulting low conduction loss and design simplicity [7]. Theoretically, the boost converter static gain tends to be infinite when duty cycle tends to unity. However, in practical terms, such gain is limited by the $I_D R$ loss in the boost inductor due to its intrinsic resistance, leading to the necessity of accurate and high-cost drive circuitry for the active switch, mainly because great variations in the duty cycle will affect the output voltage directly [8]. Due to the importance of the conventional boost converter in obtaining distinct and improved topologies for voltage step-up applications, some techniques have been developed and modified with the aim of improving the characteristics of the original structure. Basically, two strategies are adopted for this purpose: voltage step-up with and without using extreme values of duty cycle. Some arrangements available in the literature will be discussed as follows. Cascading one or more boost converters may be considered to obtain high voltage gain. Even though more than one power processing stage exists, the operation in continuous conduction mode (CCM) may still lead to high efficiency [9]. The main drawbacks in this case are increased complexity and the need for two sets that include active switches, magnets, and controllers. Besides, the controllers must be synchronized and stability is of great concern. Due to high power levels and high output voltage, the latter cascaded boost stage has severe reverse losses, with consequent low efficiency and high electromagnetic interference (EMI) levels. Typical examples of such topologies are the single-switch quadratic boost converter and the two-switch three-level boost converter. Converters with magnetically coupled inductance such as flyback or the single-ended primary inductance converter (SEPIC) can easily achieve high voltage gain using switches with reduced on-resistance, even though efficiency is compromised by the losses due to the leakage inductance. An active clamping circuit is able to regenerate the leakage energy, at the cost of increased complexity and some loss in the auxiliary circuit. A hybrid boost–flyback converter is introduced. The efficiency of the conventional flyback structure is typically low due to the parasitic inductance. A possible solution lies in connecting the output of the boost converter to that of the flyback topology, with consequent increase of voltage gain due to the existent coupling between the arrangements. In this case, the boost convert behaves as an active clamping circuit when the main switch of the flyback stage is turned OFF. A boost converter using switched capacitors is proposed, where high voltage gain can be obtained, but it is restricted to low-power applications. In this case, the dc output voltage can be increased as desired by adding a given number of capacitors. Low duty cycle is used, alleviating the problem of the boost diode reverse recovery. However, the high component count with distinct ratings is an inherent drawback. As the power rating increases, it is often required to associate converters in series or in parallel. In high-power applications, interleaving of two boost converters is usually employed to improve performance and reduce size of magnetics. Besides, for high-current applications and voltage step-up, the currents through the switches become just fractions of the input current. Interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, as the size of the energy storage inductors and differential-mode EMI filter in interleaved implementations can be reduced. The use of the 3SSC is associated with the following advantages: utilization of only
one primary winding that allows the addition of a dc current blocking capacitor in series connection, in order to avoid the transformer saturation problem; less copper and reduced magnetic cores are involved during the transformer assembly and the moderate leakage inductance of the transformer allows the reduction of overvoltage, and the commutation losses of the switches. This paper presents a topology for voltage step-up applications based on the use of multiplier cells constituted by diodes and capacitors. The converter is able to operate in overlapping mode (when a duty cycle $D$ is higher than 0.5) and nonoverlapping mode (when a duty cycle $D$ is lower than 0.5). However, the study carried out in this paper only considers the operation with $D > 0.5$. The generic structure, which is valid for any number of cells, is initially presented, while the analysis is focused on structures with three cells, aiming to determine the stress regarding the elements that constitute the aforementioned configurations. Experimental results regarding the structure with three multiplier cells are also presented and discussed to validate the proposal.

II. PROPOSED TOPOLOGIES

In the resulting cell, the controlled switches can be represented by MOSFETs, junction field-effect transistors, insulated gate bipolar transistors bipolar junction transistors, etc. All the generated topologies present bidirectional characteristics. It is possible to generate the six novel nonisolated dc–dc converters, order to better understand the operating:
1) the input voltage is lower than the output voltage;
2) steady-state operation is considered;
3) semiconductors and magnetics are ideals;
4) switching frequency is constant;
5) the turns ratio of the autotransformer is unity;
6) the drive signals applied to the switches are 180◦ displaced.

A. Operating Principle

The configuration that uses three multiplier cells is represented in Fig. 3. The equivalent circuits that correspond to the inverter operation and the relevant theoretical waveforms are presented in Figs. 4 and 5, respectively. First stage [t0, t1] [see Fig. 4(a)]: Switches $S_1$ and $S_2$ are turned ON, while all diodes are reverse biased. Energy is stored in inductor $L$ and there is no energy transfer to the load. The output capacitor provides energy to the load. This stage finishes when switch $S_1$ is turned OFF. Second stage [t1, t2] [see Fig. 4(b)]: Switch $S_1$ is turned OFF, while $S_2$ is still turned ON and diode $D_5$ is forward biased. There is no energy transfer to the load as well. Inductor $L$ stores energy, capacitors $C_1$ and $C_3$ are discharged, and capacitors $C_2$, $C_4$, and $C_6$ are charged. Third stage [t2, t3] [see Fig. 4(c)]: Switches $S_1$ and $S_2$ remain turned OFF and ON, respectively. Diodes $D_3$ and $D_7$ are forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through $D_7$. The inductor stores energy, and capacitors $C_2$ and $C_4$ are still charged. Capacitors $C_1$ is discharged, and so are $C_3$ and $C_5$.

Fourth stage [t3, t4] [see Fig. 4(d)]: Switch $S_2$ remains turned ON, diode $D_3$ is reverse biased, and diode $D_1$ is forward biased. Energy is transferred to the load through $D_7$. The inductor is discharged, and so are capacitors $C_1$, $C_3$, and $C_5$, while $C_2$ is charged.

Fifth stage [t4, t5] [see Fig. 4(e)]: This stage is identical to the first one.

III. DESIGN PROCEDURE

According to Fig. 6, the static gain of the proposed nonisolated boost converter can be further increased by adding VMCS as necessary, with consequent reduction of voltage stress across the main switches. However, this practice may lead to high component count and also compromise robustness considering that additional diodes and multiplier capacitors are included in the original topology, as seen in Fig. 3. Increased conduction and switching losses are also of major concern in this case. Even though a simpler arrangement with two VMCS could be considered instead, a design example of the proposed 3SSC boost converter with three cells is presented as follows. It will be also shown that the converter achieves high efficiency over a wide load range. The specifications are listed in Table I and were used in the implementation of an experimental prototype. Some important calculations are performed in order to evidence the loss mechanism. It is also worth to mention that both conduction and commutation losses are estimated under the rated load condition.

Sixthstage [t5, t6] [see Fig. 4(f)]: Switch $S_2$ is turned OFF and switch $S_1$ is still turned ON. Diode $D_6$ is forward biased. The inductor is charged by the input source, although capacitors $C_2$ and $C_4$ are discharged instead.

Seventh stage [t6, t7] [see Fig. 4(g)]: This stage is similar to the third one. Eighth stage [t7, t8] [see Fig. 4(h)]: Switch $S_1$ is turned ON, while $S_2$ remains turned OFF. Diodes $D_2$ and $D_8$ are forward biased, while $D_4$ is reverse biased as well as the remaining diodes. Energy transfer to the load occurs through $D_8$, and capacitor $C_6$ is still charged. The inductor is discharged, while capacitor $C_1$ is charged and capacitors $C_2$, $C_4$, and $C_6$ are discharged.
Fig. 3.1. Proposed boost converter using three VMCs.

B. Static Gain

The static gain for the generic structure of the boost converter can be obtained from the inductor volt–second balance. The voltage area multiplied by the time interval that corresponds to the inductor charge is equal to that regarding the inductor discharged. The following expression can then be derived:

\[ G_v = \frac{Vo}{Vi} = \frac{(mc + 1)}{(1 - D)} \]  

where \( mc \) is the number of voltage multiplier cells; \( Vi \) is the input voltage; \( Vo \) is the output voltage; and \( D \) is the duty cycle. Expression (1) is plotted and shown in Fig. 6, where one can see that the static gain changes when \( D < 0.5 \), as represented by the dotted line. It occurs because the multiplier capacitors are not fully charged due to the reduced charge time.

Fig. 3.2. Operating stages: (a) first stage, (b) second stage, (c) third stage, (d) fourth stage, (e) fifth stage, (f) sixth stage, (g) seventh stage, and (h) eighth stage.
Table I
Design specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tr>
<td>Rated output power</td>
<td>$P_o=1000$ W</td>
</tr>
<tr>
<td>Minimum input voltage</td>
<td>$V_{(min)}=42$ V</td>
</tr>
<tr>
<td>Maximum input voltage</td>
<td>$V_{(max)}=54$ V</td>
</tr>
<tr>
<td>Rated input voltage</td>
<td>$V=48$ V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_o=400$ V</td>
</tr>
<tr>
<td>Number of multiplier cells</td>
<td>$mc=3$</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s=25$ kHz</td>
</tr>
<tr>
<td>Maximum ripple current through inductor $L$</td>
<td>$\Delta I_L=15% I_{(max)}$</td>
</tr>
<tr>
<td>Ripple voltage through multiplier capacitors $C_1...C_6$</td>
<td>$\Delta V_{C6}=8.75% V_o$</td>
</tr>
<tr>
<td>Ripple voltage through output capacitor $C_o$</td>
<td>$\Delta V_{C0}=1% V_o$</td>
</tr>
<tr>
<td>Expected theoretical efficiency</td>
<td>$\eta=95%$</td>
</tr>
<tr>
<td>Autotransformer turns ratio</td>
<td>$\alpha=1$</td>
</tr>
</tbody>
</table>

Fig. 3.3. Normalized ripple current as a function of the duty cycle.

IV. SIMULATION

Fig. 4.1. Simulation circuit for voltage multiplier cell based universal motor

Fig. 4.2. Simulation waveform for input voltage

Fig. 4.3. Simulation waveform with ripples
V. CONCLUSION

This paper has proposed six generalized nonisolated highgain voltage dc–dc converters. To verify the principle operation of the generated structures, the boost converter was chosen. The topology is adequate for several applications such as photovoltaic systems, fuel cell systems, and UPSs, where high voltage gain between the input and output voltages is demanded.

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